REMARKS

No claims are amended. Claims 1-8 remain pending. Reconsideration and allowance of the pending claims is requested in light of the following remarks.

Request for Reconsideration and Withdrawal of the Finality of Last Office Action

Under present practice, second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement. MPEP 706.07(a).

Despite the applicant's amendment to claim 4 and new claim 7, it was indicated that the newly added feature recited in claims 4 and 7 "is considered to be met by the combination of Assaderaghi and Chen alone" (last office action, page 5, first paragraph). Thus, contrary to other statements found in the last office action, it was recognized that the new grounds of rejection was not necessitated by the applicant's amendment of the claims.

In such a situation, MPEP 706.07(a) indicates that the following office action shall not be final, and applicant requests the withdrawal of the finality of the last office action.

Claim Rejections – 35 U.S.C. § 103

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,424,011 to Assaderaghi, et al. ("Assaderaghi") in view of U.S. Patent No. 5,767,549 to Chen, et al. ("Chen"). The applicant disagrees.

Claim 1 recites a SOI layer, and it has been alleged that Assaderaghi shows SOI layers in FIGs. 5a-5l, where the SOI layers are clearly labeled "SOI".

Assaderaghi teaches that the process of forming the memory cells begins by forming the structure shown in FIG. 5a, which illustrates multiple SOI layers (labeled "SOI") that are separated by shallow isolation regions 202 (column 9, lines 61-67).

Claim 1 further recites that the SOI layer includes an active area and a device isolation area, the device isolation area including a well.

In the previous response, the applicant argued that, contrary to claim 1, "Assaderaghi contains no teaching that a device isolation area of the SOI layer includes a well." This characterization of Assaderaghi was apparently agreed upon.

The applicant further characterized Assaderaghi's shallow isolation regions 202 (FIG. 5a; column 9, lines 65-67) as corresponding to the recited device isolation area of the SOI

layer. The applicant was mistaken in this characterization of Assaderaghi, for the following reason.

Assaderaghi FIGs. 2a and 5e illustrate that the SOI layers are coextensive with the source/drain regions 20, 22. In other words, the SOI layers are located entirely in the active region that is defined by the source/drain regions 20, 22 (FIG. 2a). No part of the SOI layer is disposed in the device isolation areas, which is the region having the STIs 26, 28. Since it is well-known that SOI refers to "semiconductor on insulator" (see, e.g., column 2, line 44), and also that shallow trench isolation regions are insulative layers, it is incorrect to interpret Assaderaghi's shallow trench isolation regions 26, 28 as being included in, or part of, the SOI layer.

Furthermore, claim 1 explicitly recites that the SOI layer includes an active area and a device isolation area. The meaning of words used in a claim is not construed in a lexicographic vacuum, but ***in the context of the specification and the drawings***. MPEP 2111.02(III). The specification and drawings (see, e.g., FIG. 4B and page 7, lines 3-9) illustrate that the SOI layer 104 includes an active area 104a and a well 104b that is in the device isolation area within the SOI layer 104. In other words, the SOI layer 104 is continuous across an active region and a device isolation region. To the contrary, Assaderaghi's SOI layers stop where the STI regions begin (FIGs. 5a-5i).

Thus, not only does Assaderaghi fail to particularly teach that a device isolation area of a SOI layer includes a well, but Assaderaghi in a broader sense fails to teach that a SOI layer includes a device isolation area.

Claim 1 recites a first gate line disposed over a portion of the active area and a portion of the field oxide film.

Contrary to the above feature of claim 1, the left-most "n-gate" of FIG. 7b is not illustrated as disposed over a portion of the field oxide film. In fact, it was recognized that Assaderaghi does not teach a field oxide film as recited in claim 1. FIG. 7b also fails to show that the left-most n-gate is disposed over the STI region.

Contrary to the above feature of claim 1, the left-most "n-gate" of FIG. 8b is not illustrated as disposed over a portion of the field oxide film. In fact, it was recognized that Assaderaghi does not teach a field oxide film as recited in claim 1. FIG. 8b also fails to indicate which region corresponds to the STI region of FIG. 7b. Even accepting the premise that the STI region surrounds the active region, FIG. 8b fails to indicate which region corresponds to the active region. Thus, it is not possible to judge from FIG. 8b whether the left-most "n-gate" of FIG. 8b is disposed over a portion of the STI or not. This does not

amount to an explicit, implicit, or inherent teaching that the gate line is disposed over a portion of the field oxide film.

Claim 1 recites an insulating layer disposed on an upper surface of the active region and an upper surface of the field oxide film.

Contrary to the above feature of claim 1, it was recognized that Assaderaghi fails to teach a field oxide film as recited in claim 1. Rather, Assaderaghi teaches that the alleged insulating layer 211 (layer surrounding the second gate from the left in FIG. 5f) is disposed on an upper surface of the STI region.

Also contrary to the above feature of claim 1, the alleged insulating layer 211 is not disposed on an upper surface of the active region, it is disposed on an upper surface of the gate oxide layer 266 (FIG. 5a; column 10, lines 5-6).

Chen fails to show an insulating layer disposed on an upper surface of the active region and an upper surface of the field oxide film.

For this reason, the combination of Assaderaghi and Chen does not establish *prima facie* obviousness for claim 1 because it fails to teach or suggest all the features recited in the claim. MPEP 2143.03.

Claim 1 also recites a Local Inter-Connect (LIC) disposed in contact with the insulation layer, an upper part of a second gate line, and the active area. It should also be noted that according to claim 1, the active region runs on both side of the first gate line.

Contrary to the above feature of claim 1, nowhere does FIG. 7b, FIG. 8b, or FIGs. 5f-5L indicate that the stud interconnection 212 (FIG. 5f; column 10, lines 44-45) that rises vertically from the alleged second gate line (right-most "n-gate" of SRAM cell in FIG. 5L) is part of the same interconnect structure as the stud interconnection 212 that rises vertically from the active region surrounding the first gate line (left-most "n-gate" of SRAM cell in FIG. 5L).

Also contrary to the above feature of claim 1, nowhere does FIG. 7b, FIG. 8b, or FIGs. 5f-5L indicate that the first level metallization 213 (FIG. 5g; column 10, lines 53-54) that lies horizontally over the alleged insulation layer 211 is part of the same interconnect structure as the stud interconnection 212 that rises vertically from the alleged second gate line (right-most "n-gate" of SRAM cell in FIG. 5L) or is part of the same interconnect structure as the stud interconnection 212 that rises vertically from the active region surrounding the first gate line (left-most "n-gate" of SRAM cell in FIG. 5L).

Indeed, since the stud interconnection 212 that rises vertically from the alleged second gate line (right-most "n-gate" of SRAM cell in FIG. 5L) is connected to a P-gate (as shown in

FIG. 7b) and the stud interconnection 212 that extends vertically above the active region surrounding the alleged first gate line (left-most "n-gate" of SRAM cell in FIG. 5L) is connected to ground (as shown in FIG. 7b), the implication is that the two stud interconnections 212 are not part of the same interconnect structure.

Chen also fails to teach or suggest a Local Inter-Connect (LIC) disposed in contact with the insulation layer, an upper part of a second gate line, and the active area.

For this additional reason, the combination of Assaderaghi and Chen does not establish *prima facie* obviousness for claim 1 because it fails to teach or suggest all the features recited in the claim. MPEP 2143.03.

Claims 2-3 are allowable over the combination of Assaderaghi and Chen at least because any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03.

Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Assaderaghi in view of Chen and U.S. Patent No. 5,026,666 to Hills, et al. ("Hills"). The applicant disagrees.

Similar to claim 1, claim 4 recites a gate line disposed across the second active area and across a portion of the field oxide layer. Assaderaghi and Chen fail to disclose this feature, for the same reasons discussed above for claim 1. Furthermore, Hills is not alleged to teach this feature, nor does it do so.

Consequently, the combination of Assaderaghi, Chen, and Hills fails to establish *prima facie* obviousness for claim 4 because it does not teach or suggest all the features recited in the claim. MPEP 2143.03.

Similar to claim 1, claim 4 recites a metal fill disposed in contact with the insulation layer, an upper surface of the gate line, and an upper surface of the first active area. Assaderaghi and Chen fail to disclose this feature for the same reasons discussed above for claim 1. Furthermore, Hills is not alleged to teach this feature, nor does it do so.

Consequently, for this additional reason the combination of Assaderaghi, Chen and Hills fails to establish *prima facie* obviousness for claim 4. MPEP 2143.03.

Claim 4 additionally recites an insulation layer disposed on the first active area and disposed on the field oxide layer, the insulation layer in contact with a sidewall of the gate line.

The applicant refutes the two specific assertions made in the last office action on page 5, first paragraph, that "gate spacer layers (conformal layers 210) can reasonably be

considered to be part of the gate line or alternatively part of the insulation layer [211] (since both are typically silicon oxide)."

Gate spacer layers cannot be reasonably considered part of the gate line, since, as has been recognized, the gate spacer layers are typically insulative in nature, rather than conductive in nature as gate lines are well-known to be.

As for the second, alternate assertion, it amounts to a statement that a gate spacer is inherently part of a surrounding insulation layer because gate spacers and insulation layers are typically both made of the same material.

The applicant agrees that this may typically be the case, but it is not necessarily always the case. For example, it is known that gate spacers are often made of a different material than a surrounding insulation layer in order to achieve different etch rates and protect the gate when an etch is occurring in the surrounding insulation layer. The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. MPEP 2112(IV), emphasis in original. Thus, gate spacers cannot reasonably be considered part of a surrounding insulation layer.

Regarding the Hills reference, the fact that Hills regards the gate sidewall oxide spacers 129-130 as optional in order to provide for LDD structures (column 2, lines 25-30) does not amount to a global teaching that sidewall oxide spacers are only used for the purpose of providing LDD structures. As explained above, gate spacers may be used for purposes other than the formation of LDD structures.

Assaderaghi itself contains no indication that LDD structures are present in the source/drain regions, so Assaderaghi must teach the use of gate spacers for reasons other than to provide for the formation of LDD structures. Thus, one of ordinary skill would not be motivated to remove gate spacers from Assaderaghi merely based upon Hills teaching that they are used to form LDD structures.

Indeed, since Assaderaghi's gate spacers cannot be said to be used to form LDD structures, modifying Assaderaghi by removing the gate spacers would render Assaderaghi's gate spacers unsatisfactory for their intended purpose, and in such a case there can be no suggestion or motivation to make the proposed modification. MPEP 2143.01.

Since there is no motivation or suggestion to modify Assaderaghi with Hills in the manner that is suggested, a *prima facie* case of obviousness is not established by the combination of Assaderaghi, Chen and Hills. MPEP 2143.

Claims 5-6 are allowable over the combination of Assaderaghi, Chen and Hills at least because any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03.

Regarding claim 7, it recites features that are similar to claim 4 that were discussed above. Consequently, the comments made above regarding claim 4 apply equally as well to claim 7.

Claim 8 is allowable over the combination of Assaderaghi, Chen and Hills at least because any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03.

Conclusion

For the above reasons, reconsideration and allowance of the pending claims is requested. Please telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (571) 273-8300 on December 2, 2005.

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